**Claim Amendments**

Please amend claims 1, 2, 9-13, and 26 as follows:

Please cancel claims 15-25 as follows:

Please add new claims 27-37 as follows:

**Claims as Amended**

1. (currently amended) A method for forming a recessed gate structure with reduced current leakage and overlap capacitance comprising the steps of:

providing a silicon substrate ~~including one of N and P-well doped regions and an overlying the CVD silicon oxide~~ layer;

forming a silicon oxide layer on the silicon substrate;

forming an opening in the ~~CVD~~ silicon oxide layer to include a recessed area having about the same width as the opening extending into a thickness portion of the silicon substrate;

then lining the opening sidewalls and recessed area sidewalls with at least one dielectric

liner followed by forming an exposed silicon substrate portion at a bottom portion of the recessed area having a width smaller than the opening;

then thermally growing a gate oxide over the exposed silicon substrate portion[[s]] of the recessed area;

backfilling the opening with polysilicon;

planarizing the polysilicon to the opening level to reveal the silicon oxide layer; and,

selectively removing the silicon oxide layer to form a recessed gate structure.

2. (currently amended) The method of claim 1, ~~further including steps following the step of forming an opening and prior to the step of thermally growing a gate oxide comprising~~ wherein the step of lining the opening comprises:

thermally growing a first silicon oxide ~~layer~~ liner comprising the at least one dielectric liner to line the recessed area;

~~blanket depositing~~ forming a silicon nitride ~~layer~~ liner comprising the at least one ~~dielectric liner over the opening~~ to include lining the opening and recessed area ~~and overlying~~ on the first silicon oxide ~~layer~~ liner; and,

etching the silicon nitride ~~layer~~ liner and the first silicon oxide ~~layer~~ liner at a bottom portion of the opening to form the exposed silicon substrate portion[[s]] ~~having a width smaller~~ than the opening;.

3. (original) The method of claim 1, wherein the recessed area is formed having a recessed depth of from about 200 Angstroms to about 400 Angstroms measured from the silicon substrate surface.

4. (original) The method of claim 1, further comprising the step of forming a source/drain extension (SDE) doped regions adjacent either side of the recessed gate structure.

5. (original) The method of claim 4, wherein the SDE doped regions are formed by one of an ion implant and a plasma immersion doping process.

6. (original) The method of claim 4, wherein the depth of the SDE doped regions measured from

the silicon substrate surface to a lowermost portion of the SDE doped region is less than about 1200 Angstroms.

7. (original) The method of claim 6, wherein the depth of the recessed area is from about 1/3 to about 1/6 of the depth of the SDE doped regions.

8. (original) The method of claim 1, wherein the gate oxide layer thickness is less than about 50 Angstroms.

9. (currently amended) The method of claim 2, wherein the first silicon oxide ~~layer~~ liner thickness is less than about 50 Angstroms.

10. (currently amended) The method of claim 2, wherein the silicon nitride ~~layer~~ liner thickness is between about 50 Angstroms and about 200 Angstroms.

11. (currently amended) The method of claim 2, wherein the step of etching comprises a dry anisotropic etching step for etching the silicon nitride ~~layer~~ liner.

12. (currently amended) The method of claim 2, wherein the step of etching comprises a wet

etching process for etching the first silicon oxide ~~layer~~ liner.

13. (currently amended) The method of claim 1, further comprising the steps of forming sidewall spacers adjacent either side of the recessed gate structure and forming source/drain (S/D) doped regions.

14. (original) The method of claim 13, further comprising the step of forming self aligned silicide (salicide) portions adjacent the sidewall spacers.

claims 15-25 cancelled

26. (currently amended) A method for forming a recessed gate structure having reduced current leakage and overlap capacitance comprising the steps of:

providing a silicon substrate ~~including one of N and P-well doped regions and an overlying the CVD silicon oxide layer~~;

forming a silicon oxide layer on the silicon substrate;

then forming an opening in the ~~CVD~~ silicon oxide layer to include a recessed area having about the same width as the opening extending into a thickness portion of the silicon substrate;

then growing a first silicon oxide ~~layer~~ liner to line the recessed area;

then ~~blanket depositing~~ forming a silicon nitride ~~layer~~ liner over the opening to include lining the opening and recessed area ~~overlying~~ on the first silicon oxide layer liner;

then etching the silicon nitride ~~layer~~ liner and the first silicon oxide ~~layer~~ liner at a bottom portion of the opening to form an exposed silicon substrate portion having a width smaller than the opening;

then thermally growing a gate oxide over the exposed silicon substrate portion;

backfilling the opening with polysilicon;

planarizing the polysilicon to the opening level to reveal the silicon oxide layer; and,

then selectively removing the silicon oxide layer to form a recessed gate structure~~; and~~;

~~forming Source/drain extension (SDE) doped regions adjacent either side of the recessed gate structure.~~

27. (new) A method for forming a recessed gate structure with reduced current leakage and overlap capacitance comprising the steps of:

providing a semiconductor substrate;

forming a first dielectric layer on the semiconductor substrate;

then forming an opening in the first dielectric layer extending into a thickness portion of the semiconductor substrate to form a recessed area having about the same width as the opening;

then lining the opening including the recessed area with at least a second dielectric liner;

then removing a portion of the at least a second dielectric liner at a bottom portion of the recessed area to expose the semiconductor substrate, said exposed bottom portion having a width smaller than the opening;

then forming a gate dielectric layer over said exposed bottom portion;

then backfilling the opening with a gate electrode material;

then planarizing the polysilicon to the opening level to reveal the first dielectric layer; and,

then selectively removing the first dielectric layer to form a recessed gate structure.

28. (new) The method of claim 27 wherein the first dielectric liner comprises silicon oxide grown to line the recessed area.

29. (new) The method of claim 27 wherein the gate dielectric comprises silicon oxide grown on said bottom portion.

30. (new) The method of claim 27 wherein the at least a second dielectric liner comprises a first liner of silicon oxide lining the recessed area and a second liner of silicon nitride lining the recessed area on the first liner and on the opening sidewalls.

31. (new) The method of claim 27, wherein the recessed area is formed having a recessed depth of from about 200 Angstroms to about 400 Angstroms.

32. (new) The method of claim 27, further comprising the step of forming a source/drain extension (SDE) doped regions adjacent either side of the recessed gate structure.

33. (new) The method of claim 31, wherein the SDE doped regions are formed by one of an ion implant and a plasma immersion doping process.

34. (new) The method of claim 31, wherein the depth of the SDE doped regions measured from the silicon substrate surface to a lowermost portion of the SDE doped region is less than about 1200 Angstroms.

35. (new) The method of claim 31, wherein the depth of the recessed area is from about 1/3 to about 1/6 of the depth of the SDE doped regions.

36. (new) The method of claim 27, wherein the gate dielectric layer thickness is less than about 50 Angstroms.

37. (new) The method of claim 27, wherein the gate electrode material comprises polysilicon.

THIS PAGE BLANK (USPTO)